JIS College of Engineering
Department of Electronics & Communication Engineering
Course Name Course Name: VLSI & Microelectronics Lab
Course Code: EC691 Contact: 0:0:3
Credit: 1.5

List of Experiments:

1. Simulation of CMOS inverter to plot voltage transfer characteristics (VTC) for different values of kn/kp ratio for VDD=1 V and nano dimensional channel length using SPICE.
a. Measurement Of Critical Voltages VIL, VIH,VOL, VOH fromVTC.
b. Calculation of Of noise margin from critical voltages.
2. Functional Verification, measurement of gate delay and average power consumption of CMOS inverter circuit for VDD range 0.5 V to 1.2 V and with the nano dimensional channel length of MOS transistor using pSPICE tools.
3. Design and testing of functionality of the following gate and combinational circuit with the helpof SPICE tools at schematic level.
a. CMOS AND/NAND,OR/NOR, XOR/XNORgate
b. CMOS full adder circuit.
4. Layout design and functional verification ofCMOS inverter, CMOS NAND, CMOS NOR gate using layout design tools of SPICE based design rules.
5. Design and examination of functionality ofthe sequential circuits -CMOS SRlatch, clocked SRlatch &D flip-flopat schematic level usingSPICEtools .
6. Design And simulation ofa) Logic gates) Full adder using half adders) 4:1MUX using 2:1 MUX with the help of VHDL following suitable modelling style(structural, behavioural, dataflow, mixed).
7. Design of the following Sequential circuits using VHDL
a. S-R Flip-Flop
b. 8 bit synchronous counter
c. 8Bitbi-directionalregister with tri-stated input output.
8. Familiarity with FPGA based system design. Design and realization of 4:1 Muxusing FPGA.
9. Design of CMOS differential amplifier at schematic level with active load and current mirror bias circuit for given specifications using SPICE tools.
10. Innovative Experiment.